HW#4 (Due 11/27)

1. Consider the following code sequence for a 5-stage RISC-V pipeline with split instruction cache and data cache.

sub x20,x12,x7

sub x21,x13,x8

sub x22,x14,x9

sub x23,x15,x10

ld x6,12(x4);

ld x8,16(x4);

ld x12,20(x4);

ld x15,24(x4);

add x5,x6,x8;

ld x10,20(x4);

add x1,x10,x5;

add x2,x10,x9;

add x2,x13,x2;

add x2,x15,x2;

and x11,x12,x15;

or x16,x13,x17;

or x11,x11,x16;

sd x1,24(x4);

sd x2,28(x4);

sd x11,32(x4);

Suppose the clock cycle time is 1ns. The hit time is 1 clock cycle. The miss penalty is 200 clock cycles.

1. Determine the number of memory accesses of the code sequence.
2. Suppose there are 2 misses for instruction accesses, and 1 miss for data accesses. Determine the miss rates for instruction cache and data cache, respectively.
3. Determine the average memory access time (in ns) of the instruction cache and data cache, respectively.
4. Determine the percentage of the memory accesses which are instruction accesses. Determine the percentage of the memory references which are data accesses.
5. Determine the average memory access time (in ns) for the code sequence.